REMARKS

Claims 1, 2, 5-9, 12-17, 19, 21-23, 25-31, 33-38, and 40-43 are pending. Claims 1, 5, 8, 12, 15, 21, 23, 25-28, 30, 33, 37, and 40 have been amended. Claims 3, 4, 10, 11, 18, 20, 24, 32, and 39 have been cancelled. Reexamination and reconsideration of the application are respectfully requested.

The Examiner rejected claims 1, 2, 4, 8, 9, 11, and 15 under 35 U.S.C. §102 (a) as being anticipated by Kim, U.S. PG. 2004/0093461 (hereinafter the Kim reference). The Examiner rejected claims 6 and 13 under 35 U.S.C. §103 (a) as being obvious over the Kim reference. The Examiner rejected claims 16, 17, 19, 20, and 22 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of Zheng, U.S. Patent No. 6,195,303 (hereinafter the Zheng reference). The Examiner rejected claims 3, 7, 10, 14, 24, 25, 27-32, 34-39, and 41-43 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of Proebsting, U.S. Patent No. 6,871,261 (hereinafter the Proebsting reference). The Examiner rejected claims 18, and 23 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of the Zheng reference, and further in view of the Proebsting reference. The Examiner rejected claims 5, and 12 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of Tsern et al., U.S. Patent No. 6,075,744 (hereinafter the Tsern reference). The Examiner rejected claim 21 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of the Zheng reference, and further in view of the Tsern reference. The Examiner rejected claims 26, 33, and 40 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of the Proebsting reference, and further in view of the Tsern

reference. The above 35 U.S.C. §103 (a) rejections with respect to the Tsern reference are respectfully traversed.

Claim 5 rewritten in independent form recites:

A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command.

The Examiner rejected claims 5, and 12 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of Tsern et al. The Examiner rejected claims 26, 33, and 40 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of the Proebsting reference, and further in view of the Tsern reference. The Examiner rejected claim 21 under 35 U.S.C. §103 (a) as being obvious over the Kim reference, in view of the Zheng reference, and further in view of the Tsern reference.

Applicant has slightly amended and rewritten claims 5, 12, 21, 26, 33, and 40 in independent form. In rejecting claim 5, the Examiner stated "with respect to claim 5, Kim teaches all other limitations of the parent claim but fails to teach that multiple rows per memory bank array are refreshed in a staggered fashion. Tsern et al. teach a method of refreshing a memory bank array wherein multiple rows per memory bank

array are refreshed in a staggered fashion per the auto-refresh command, in col. 5, lines 6-18."

The Tsern reference does not show "initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command."

The Tsern reference states that "FIG. 1 shows a typical current profile 10 over time for **a row** sense operation. At a point 12, there is a large initial spike of current near time 0. This spike is large because **the row** sensing circuits have been designed to access cell data as quickly as possible in order to minimize the latency to the first allowable page access to bits stored in the sense amps." (Col. 4, lines 3-9, emphasis added). The Tsern reference states that "with multiple banks simultaneously doing **a row** sense, the current spike effect can be additive, thus causing greater probability of circuit failure." (Col. 4, lines 14-16, emphasis added).

The Tsern reference states that "the transitioning of the voltage levels SAP and SAN to their high and low levels as shown in FIG. 5 is what causes the current spike illustrated in FIG. 1. A similar current spike can be caused by the precharge equalization transistor. FIG. 6A is a circuit diagram of one embodiment of the invention for **modifying sense amp driver transistor 30** to reduce the voltage spike. The sense amp driver transistor 30 (FIG. 4) is replaced by three driver transistors 48, 50 and 52 in parallel. By **sequentially turning on these transistors**, the current spike can be spread out as illustrated in FIG. 6B. FIG. 6B shows a first waveform SAN0 which will turn on transistor 48 at a time 54." (Col. 4, line 59 - Col. 5, line 3, emphasis added).

The Tsern reference states that "this results in the waveform 60 of FIG. 6B, which has three smaller peaks 62, 64 and 66, instead of the combined current peak of a single transistor. The three transistors can either be of the same size, or different sizes. The first transistor turned on could be the largest transistor, or the smallest. The **staggered turn-on** would be used for refresh operations only, such as simultaneous multibank refresh, with all three transistors being simultaneously turned on for a normal access operation." (Col. 4, lines 14-16, emphasis added).

The Tsern teaches modifying sense amp driver transistor 30 to reduce the voltage spike. This is accomplished by replacing the sense amp driver transistor 30 (FIG. 4) by three driver transistors 48, 50 and 52 in parallel. By sequentially turning on these transistors, the current spike can be spread out. The sense amp drive transistor and the three driver transistors 48, 50 and 52 in parallel access one cell of a single row during a refresh operation. The three driver transistors 48, 50 and 52 in parallel sequentially turned on when accessing one cell of a single row during a refresh operation.

Therefore, the Tsern reference does not show "initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command."

Accordingly, the Applicant respectfully submits that rewritten independent claim 5 distinguishes over the above-cited references.

Rewritten independent claims 12, 21, 26, 33, and 40 recite limitations similar to rewritten independent claim 5. Specifically, claims 12, 21, 26, 33, and 40 recite "wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command". Therefore, Applicant respectfully submits that claims 12, 21, 26, 33, and 40 distinguish over the above-cited references for the same reasons as set forth above with respect to rewritten independent claim 5.

Independent claim 1, as amended, recites:

A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

The Examiner rejected claims 1, 2, 4, 8, 9, 11, and 15 under 35 U.S.C. §102 (a)

as being anticipated by the Kim reference.

The Kim reference, the Zheng reference, the Proebsting reference, and the Tsern reference do not disclose, teach, or suggest the method specified in independent claim 1, as amended. Unlike the method specified in independent claim 1, as amended, the Kim reference, the Zheng reference, the Proebsting reference, and the Tsern reference do not show that "multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation."

As discussed above in relation to claim 5, the Kim reference, the Zheng reference, the Proebsting reference, and the Tsern reference do not show that "multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command. In addition, the Kim reference, the Zheng reference, the Proebsting reference, and the Tsern reference do not show that "the second operation begins after all the rows have begun the auto refresh operation."

Accordingly, Applicant respectfully submits that independent claim 1, as amended, distinguishes over the above-cited reference. Claims 2, 6, and 7 depend directly or indirectly from independent claim 1, as amended. Therefore, Applicant respectfully submits that claims 2, 6, and 7 distinguish over the above-cited references for the same reasons as set forth above with respect to independent claim 1, as amended.

Independent claims 8, 15, 30, and 37, as amended, recite limitations similar to independent claim 1, as amended. Specifically, independent claims 8, 15, 30, and 37, as amended, recite that "multiple rows per memory bank array are refreshed in a

staggered fashion per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation."

Accordingly, Applicant respectfully submits that independent claims 8, 15, 30, and 37, as amended, distinguish over the above-cited references. Claims 9, 13, and 14 depend directly or indirectly from claim 8, as amended. Claims 16, 17, 19 depend directly or indirectly from claim 15, as amended. Claims 31, and 34-36 depend directly or indirectly from claim 30, as amended. Claims 38, and 41-43 depend directly or indirectly from claim 37, as amended. Therefore, Applicant respectfully submits that claims 9, 13, 14, 16, 17, 19, 31, 34-36, 38, and 41-43 distinguish over the above-cited references for the same reasons as set forth above with respect to independent claim 1, as amended.

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Applicant believes that the foregoing amendment and remarks place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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Date: June 7, 2006

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